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COMPARISON OF THE Ti/n-GaAs SCHOTTKY CONTACTS' PARAMETERS FABRICATED USING DC MAGNETRON SPUTTERING AND THERMAL EVAPORATION

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We have fabricated the Ti/n-type GaAs Schottky diodes (SDs) by the DC magnetron deposition and thermal evaporation, cut from the same GaAs substrates, and we have made a comparative study of the current–voltage (I–V) measurements of both SDs in the measurement temperature range of 160–300 K with steps of 10 K. The barrier height (BH) values of about 0.82 and 0.76 eV at 300 K have been obtained for the sputtered and evaporated SDs, respectively. It has been seen that the apparent BH value for the diodes has decreased with decreasing temperature obeying the single-Gaussian distribution (GD) for the evaporated diode and the double-GD for the sputtered diode over the whole measurement temperature range. The increment in BH and observed discrepancies in the sputtered diode have been attributed to the reduction in the native oxide layer present on the substrate surface by the high energy of the sputtered atoms and to sputtering-induced defects present in the near-surface region. We conclude that the thermal evaporation technique yields better quality Schottky contacts for use in electronic devices compared to the DC magnetron deposition technique.

Keywords: Schottky diode; barrier inhomogeneity; GaAs; current-voltage characteristics; Gaussian distribution.

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1. Introduction

The electrical properties of metal-semiconductor contacts are widely studied due to their basic physical properties and their technological applications. Schottky diodes (SDs) are the basis of large number of compound semiconductor electronic devices, including microwave diodes, field-effect transistors (FETs), metal-semiconductor field effect transistors (MESFETs), metal-insulator semiconductor field effect transistors (MISFETs), semiconductor detectors, varactors, switching devices, microwave devices, light emitting diodes (LEDs), solar cells and photo detectors.[1–10]

High quality GaAs-based Schottky contacts are very important for devices such as MESFETs and high-electron mobility transistors (HEMTs) which

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are used in digital, microwave, and optical detection systems.[4,6] It is well-known that the Schottky barrier height (SBH) depends, amongst others, upon the quality of the semiconductor material, the method of surface preparation prior to metallization and the metallization itself.[1,11,12] The interface quality between a semiconductor and a deposited metal has considerable influence on the electrical properties of a SD. Therefore, to what degree this dependence holds varies considerably depending on the metallization technique of the contacts and the crystal quality of the GaAs itself. Particularly, native defects such as EL2 can also be a factor for the crystal quality.[13,14] It has been reported in the literature that different metal deposition techniques may introduce varying levels of damage into a semiconductor surface region during metal deposition.[8,15,16]

Di Dio *et al.*[9] have investigated temperature-dependent forward and reverse current–voltage (I–V) characteristics of Ti/GaAs diodes prepared by ion beam sputtering. They have discussed the correlation between the different sputtering preparation conditions and current transport mechanism. They have reported that the thermionic emission (TE) is the main current-transport mechanism for all the samples, but the diodes show a deviation from this behavior at low temperatures. Arulkumaran *et al.*[10] have analyzed electrical characteristics of Ti/n-GaAs SDs formed by the physical vapor evaporation technique and obtained a barrier height (BH) of 0.78 eV and an ideality factor of 1.25 for these diodes. Ayyildiz and Türüt[17] have studied the effect of thermal treatment on the characteristic parameters of Ni/-, Ti/- and NiTi alloy/n-GaAs SDs formed by the physical vapor evaporation technique. The values of the ideality factor and BH of as-deposited Ti/n-GaAs SDs were found to be 1.08 and 0.64 eV, respectively. Sehgal *et al.*[18] have investigated the electrical characteristics of Ti/Pt/Au/n-GaAs Schottky contacts prepared by electron beam (EB) deposition and RF sputtering. The values of current BH were found to be 0.85 eV and 0.67 eV for the EB and RF3 Schottky contacts, respectively. In the literature,[8,15,16] the electrical properties of semiconductor devices are reported to be strongly influenced by the presence of electrically active defects introduced during metal deposition.

Our purpose is to compare the characteristic diode parameters of the Ti/n-GaAs SDs prepared by DC magnetron sputtering deposition with those of the SDs prepared by the thermal evaporation techniques. The analysis of the I–V characteristics of the MS rectifying contacts at only one measurement temperature does not give us enough information about different aspects of the temperature-dependent conduction mechanisms. Therefore, the I–V measurements of the SDs were made in the measurement temperature range of 160–300 K with steps of 10 K. The values of the apparent BH and the ideality factor were obtained from the forward biased I–V curves by using the TE theory. To the best of our knowledge, a comparative study of sample temperature-dependent I–V characteristics of the sputtered and evaporated Ti/n-GaAs SDs have not been reported over a wide temperature range of 160–300 K in literature so far. The temperature dependence of the SBH of the fabricated diodes was interpreted on the basis of the existence of the GD of the SBHs around mean values due to SBH inhomogeneities at the MS interface.

2. Experimental Procedure

The Te-doped n-GaAs substrate with a carrier concentration of 2-5 $\times 10^{17}$ cm^{-3} grown by the liquid-encapsulated Czochralski (LEC) method was cleaned consecutively with acetone, methanol, trichloroethylene, deionised water (18 MΩ) 5 min using ultrasonic agitation in each step to remove organic contaminations. Then, the substrate was immersed in an HCl:H_2O (1:1) solution to get rid of the native oxide on the GaAs surface, washed with de-ionized water and dried with high-purity nitrogen gas. The substrate was inserted into the deposition chamber immediately after the etching process. The ohmic contacts were formed by thermal evaporation of Au–Ge (88% Au, 12% Ge) on unpolished sample at 5×10^{-6} Torr base pressure and annealed at 450°C for 3 min in flowing high purity (6N) argon gas in a quartz tube furnace. The sample was cut into two pieces of 10×10 mm^2. One of them was immediately inserted into the evaporation chamber to form Schottky contacts by DC magnetron sputter technique. Sputtering conditions were flow of Ar (5N purity) with a 12 ccm/min (maintained by a digital mass flow controller), sputter head with a power density of 3 W/cm^2, current was a 0.2 A and the background pressure was 14 mTorr. Also, before

30 nm Ti deposition process, a pre-sputtering of the Ti target (4N purity) was carried out to remove surface contamination. Deposition rate of Ti was a 0.5 Å/s. Next, 50 nm Au (4N purity) was evaporated thermally, deposition rate was 1.0 Å/s and background pressure was better than 1×10^{-6} Torr. The Schottky contacts were formed by evaporating the titanium and gold metal dots with diameter of about 1.0 mm.

In second piece of GaAs, Schottky metallization was performed as follows: Ti (5N purity) filament was used to 30 nm Ti deposition. Deposition rate of Ti was 0.4 Å/s and background pressure were better than 1×10^{-6} Torr. Next, 50 nm Au (4N purity) was evaporated thermally with the same conditions in sample MS. Background pressure, gas flow rate, deposition rate and other metallization process were kindly controlled with vacuum gauges, digital mass flow controller and QCM thickness monitor. All contact metals were deposited in the same environment without breaking the vacuum using a high vacuum metallization system (NANOVAK-NVTS400).

The *I–V* measurements of the Ti/*n*-GaAs SCs were accomplished by employing a computer-controlled HP 4140B picoamperemeter and liquid nitrogen cooled cryostat in the temperature range of 160–300 K by the steps of 10 K in the dark. The temperature accuracy is better than ±1 K during each temperature point of measurement.

3. Results and Discussion

Figure 1 shows a comparison of the *I–V* characteristics at some measurement temperatures for the Ti/*n*-GaAs SBD prepared by the DC magnetron sputtering deposition with those for the Ti/*n*-GaAs SBD prepared by the thermal evaporation deposition.

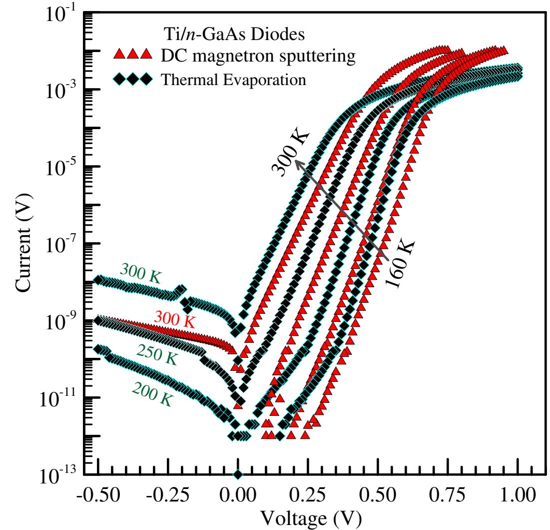

Fig. 1. (Color online) Comparison of the current–voltage characteristics at some measurement temperatures for the Ti/*n*-GaAs SDs prepared by the DC magnetron sputtering and thermal evaporation deposition.

Table 1 shows some diode parameters from the forward bias *I–V* characteristics for both diodes at these temperatures, where R_S is the series resistance, Φ_b is zero bias BH, n is ideality factor which introduces a measure of the deviation of the experimental *I–V* data from the ideal TE model. When the linear portions of the forward bias *I–V* curves in Fig. 1 are considered at each temperature, the thermal evaporated diode (TED) exhibits a higher forward current compared to the DC magnetron sputtered diode (MSD). Recent investigations have shown that the sputtering deposition generates defects into the semiconductor substrate.[15,16] The generated states in the surface region of the GaAs substrate during bombardment may be responsible for the observed

Table 1. Some diode parameters from the current–voltage characteristics for both diodes at these temperatures, R_S(Q): the series resistance, Φ_b (eV): zero bias BH, n: ideality factor.

	Thermal evaporation			DC magnetron sputtering		
T(K)	n	Φ_b (eV)	R_S (Ω)	n	Φ_b(eV)	R_S(Ω)
300	1.104	0.756	159.44	1.102	0.817	15.76
250	1.152	0.763	155.65	1.129	0.817	24.26
200	1.214	0.731	167.03	1.245	0.773	25.84
160	1.294	0.690	174.01	1.474	0.676	22.28

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electrical behavior.[12,19] In spite of this, as can be seen from Fig. 1, the forward bias I–V curves of the TED device shows more downward curvature than those of the MSD device in high bias voltage region. As well-known, the downward curvature region in the forward bias I–V curves at high bias voltage arises from the series resistance, R_S, of the neutral region of the semiconductor bulk between the depletion region and ohmic contact. The series resistance values were calculated using a method developed by Cheung and Cheung[20] obtained from the following forward bias TE current equation.[1–3] As can be seen from Table 1, the TED device has the R_S values of 159.44 Ω and 174.01 Ω, while the MSD device has the R_S values of 15.76 Ω and 22.28 Ω at 300 K and 160 K, respectively. The series resistance of an intimate MS contact without interfacial layer must only come from the semiconductor bulk. The larger value than that expected for R_S may be supplied from the contribution of the imperfect ohmic contact plus native oxide layer on the semiconductor surface to the neutral region series resistance.

It has been reported that the preparation of clean surfaces takes place during sputter deposition because of the chemical reactivity of the high energy of the sputtered atoms.[12,19] This process may have a very large effect on the native oxide layer exist on semiconductor surface and thus, on the mechanism of current transport. Therefore, as stated in,[12,19] the sputtering can help to remove the native oxide layer and to increase the diode quality. Thereby, it can be said that the high R_S value arises from the native oxide layer plus semiconductor bulk and imperfect ohmic contact resistances. The contribution of the ohmic contact resistance to the series resistance must be too small to change the series resistance of the device.[1–3] The series resistance of the device should only come from the neutral region of the semiconductor substrate. The series resistance of the GaAs bulk substrate can be calculated from $R_B = (\rho L)/\mathrm{A}$, where $\rho = 0.0075\,\Omega$-cm and $L = 450 \pm 25\,\mu$m and $A = 7.85 \times 10^{-3}\,\mathrm{cm}^2$ are the resistivity and bulk thickness of the GaAs and the area of the Schottky contact. A value of about $0.435 \pm 0.025\,\Omega$ for R_B was obtained. Thus, it can be said that the contribution of the ohmic contact resistance to the series resistance of both diodes is about $15.325 \pm 0.025\,\Omega$ because the series resistance value of the MSD device without the native oxide layer was about 15.76 Ω.

Using the TE current equation, the effective or apparent BH and ideality factor n values can be calculated from the intercept and slope of the linear portion of the forward bias I–V curves at each temperature in Fig. 1. The TE I–V equation for a forward biased SD is given as follows.[1–3]

$$I = I_S\left[\exp\left(-\frac{q(V - IR_s)}{nkT}\right) - 1\right], \quad (1)$$

where I_S is the saturation current and is written as

$$I_S = AA^*T^2\exp\left(-\frac{\Phi_{b0}}{kT}\right) \quad (2)$$

and $A*$ is the effective Richardson constant of $8.16\,\mathrm{Acm}^{-2}\mathrm{K}^{-2}$ for n-type GaAs, A is the diode area. R_S is the series resistance of the neutral region of the semiconductor substrate between the depletion region and ohmic contact. $(V - IR_S)$ and $\mathrm{IR_S}$ are the voltage drop across the depletion region and series resistance, respectively. From Eqs. (1) and (2), respectively, the ideality factor n and the effective BH Φ_{b0} at zero bias are written as

$$n = \frac{q}{kT}\ln\left(\frac{dV}{d\ln I}\right) \quad (3)$$

and

$$\Phi_{\mathrm{ap}} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right). \quad (4)$$

The ideality factor n accounts for the departure of the current transport mechanisms from the ideal TE model. The ideality factor and BH values for both diodes were calculated using Eqs. (3) and (4) at each measurement temperature, respectively. The values at some temperature are given in Table 1. The BH for the sputtered and evaporated SDs has taken the values of 0.817 eV and 0.756 eV at 300 K and 0.773 eV and 0.731 eV at 170 K and 0.639 eV and 0.676 eV at 160 K, respectively. The ideality factor for the sputtered and evaporated SDs has been obtained as 1.102 and 1.104 at 300 K and 1.129 and 1.152 at 170 K and 1.474 and 1.294 at 160 K, respectively. Ejderha *et al.*[19] have obtained a BH value of 0.80 eV with an ideality factor value of 1.04 (300 K) for the DC magnetron sputtered Ti/n-GaAs which is in close agreement with the value of 0.817 eV obtained for the sputtered diode by us.

As can be seen, the BH due to sputtering increases at each temperature except for 160 K. That is, the

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sputtered Ti/n-GaAs diode exhibited a higher BH compared to the evaporated Ti/n-GaAs diode, as can be seen in Table 1. It is supposed that the surface states in the surface of the GaAs substrate region during bombardment are responsible for this electrical behavior.[12,19] The sputtering may cause to defect-induced interface states within the band gap of the semiconductor at metal-semiconductor interfaces. The space charge change in the underlying semiconductor substrate and thus BH change depend on the presence of the positive or negative charges in the interface states between the rectifying contact metal and semiconductor substrate.[2,3,19] For n-type semiconductor substrates, the presence of negatively charged acceptors in the interface states at the rectifying MS contact interface increases the BH compared to the case when no interface defects are present because the positive space charges in the depletion region of the metal/n-type semiconductor rectifying contact will increase and thus the BH.[2,3,19]

It is shown experimentally in the literature that the ideality factor of a SD increases when the measurement temperature is decreased, and thus, there are many different temperature dependences of the ideality factor. Therefore, the deduced BH and ideality factors are found to vary with change of the measurement temperature. This case generally is known as the T_0 anomaly.[2,3,21–24] In such a case, for $q(V - IR_s) \geq 3\,kT$, Eq. (1) can be organized as follows[2,3,21–24]

$$I = AA^{*}T^{2}\exp\left(-\frac{\Phi_{b0}}{k(T+T_0)}\right)\left[\exp\left(\frac{q(V-IR_s)}{k(T+T_0)}\right)\right], \quad (5)$$

where T_0 is a constant. When considering Eqs. (1) and (5), it arises as $nT = (T + T_0)$. It has been stated in the literature[2,21,22] that nT vs T plot related to the T_0 anomaly is used to determine the dominant conduction mechanism across the device, the TE or the thermionic field emission (TFE). Nevertheless, some authors[3,21,22] state that BH inhomogeneity offers an excellent explanation of the T_0 anomaly. Figure 2 shows nT vs T plots, according to the equation $nT = (T + T_0)$, for the evaporated SD (closed circles) and the sputtered SD (closed squares)in the temperature range of 160–300 K with steps of 10 K. The dashed straight lines show the ideal behavior line obeying TE current mechanism and the fit straight line to experimental data. The experimental data of

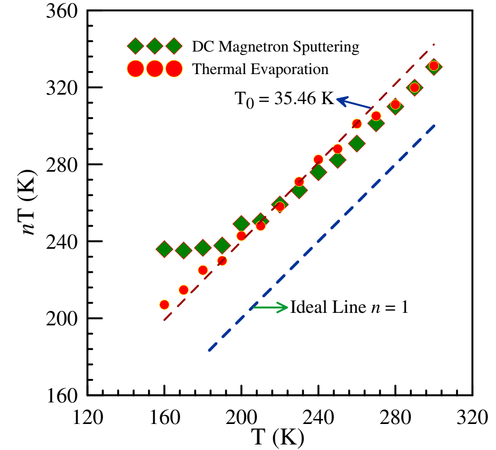

Fig. 2. (Color online) nT vs T plots in the measurement temperature range of 160–300 K with steps of 10 K, for the Ti/n-GaAs SDs prepared by the DC magnetron sputtering and thermal evaporation deposition. The dashed line fitted to experimental data is parallel to the ideal behavior line and gives a value T_0 of 35.46 K.

the considering device should lie parallel to the ideal behavior line. The dashed line fitted to the experimental data of the thermal evaporated SD is parallel to the ideal behavior line and gives a T_0 value of 35.46 K. As can be seen from Fig. 2, the shape of the experimental nT vs T curve of the sputtered SD is usually attributed to the possibility TFE current mechanism over whole temperature range. This may be related to the doping level and the distribution of the apparent BH.[21–26] As mentioned above, the sputtering may cause the defect-induced interface states at the GaAs surface. The presence of negatively charged acceptor-like interface states at the rectifying MS contact increases the positive space charges in the depletion region compared to the case when no interface defects are present.[2,3,21,22,27] In spite of this explanation by us, as mentioned also by some authors,[21,22,27] even though tunneling should dominate the carrier conduction in diodes heavily doped semiconductor substrate, the temperature dependence of the ideality factor does not provide a determination for the conduction mechanism. By considering explanations above related to the barrier inhomogeneity, we can say that the barrier inhomogeneity offers an excellent explanation of the T_0 anomaly.

Figure 3 shows the Richardson plots, in the measurement temperature range of 160–300 K with steps

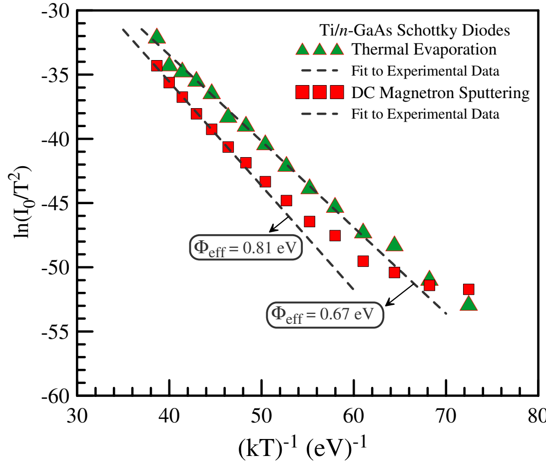

Fig. 3. (Color online) Richardson plots in the measurement temperature range of 160–300 K with steps of 10 K, for the Ti/n-GaAs SDs prepared by the DC magnetron sputtering and thermal evaporation deposition.

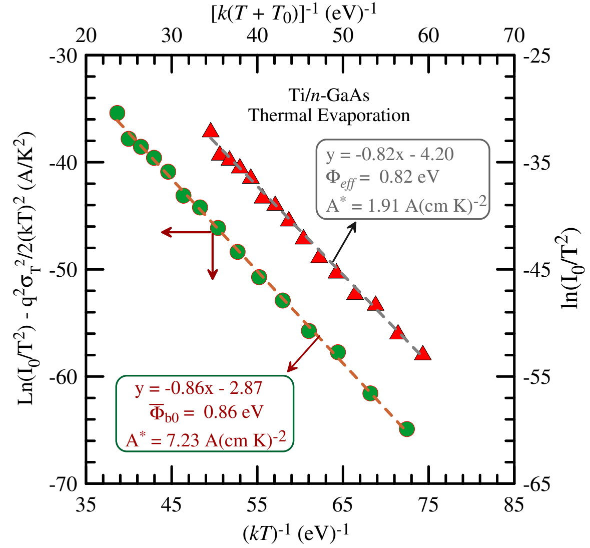

Fig. 4. (Color online) The closed circles represent modified Richardson plot according to single GD and the closed triangles circles represent modified Richardson plot according to T_0 anomaly, in the measurement temperature range of 160–300 K with steps of 10 K, for the Ti/n-GaAs SD prepared by the thermal evaporation deposition. The dashed lines represent the fits to experimental data.

of 10 K, for the sputtered (closed squares) and thermal evaporated (closed triangles) Ti/n-GaAs SDs. The effective BH value of about 0.81 eV and 0.67 eV for the sputtered and thermal evaporated SDs was obtained from the fit to the linear portion of the experimental $\ln(I_0/T^2)$ vs $(kT)^{-1}$ curves of both diodes at high temperatures. An effective BH of 0.81 eV for the sputtered SD forms the experimental $\ln(I_0/T^2)$ vs $(kT)^{-1}$ is the such as value of 0.817 eV at 300 K. The deviation in the Richardson curves, $\ln(I_0/T^2)$ vs $(kT)^{-1}$, of both diodes at low temperatures may be due to the spatially inhomogeneous BHs and potential fluctuations at the interface, that is, the current through the diode will flow preferentially through the lower barriers in the potential distribution. The closed circles in Fig. 4 represent the modified Richardson plot for the thermal evaporated SD, according to T_0 anomaly, that is, the experimental ln (I_0/T^2) vs $[k(T+T_0)]^{-1}$ plot using Eq. (5) for $(V - IR_S) = 0$. The values of about 0.82 eV and 1.91 A/cm^{2}K^2 for the effective BH and Richardson constant, respectively, were calculated from the modified Richardson plot (Fig. 4) for the evaporated SD. The value of 1.91 A/cm^{2}K^2 is 4.27 times lower than the value of 8.16 A/K^{2}cm^2 given for n-type GaAs in the literature. The $[k(T+T_0)]^{-1}$ instead of $(kT)^{-1}$ in the Richardson plot is used to modify the experimental data and thus to obtain values close to expected Richardson constant and effective BH values. Therefore, it has been seen that the effective BH value of 0.82 eV from this plot for the evaporated SD is in close agreement with the value of 0.81 eV from the $\ln(I_0/T^2)$ vs $(kT)^{-1}$ plot and value of 0.817 eV at 300 K for the sputtered SD which gives nearly ideal I–V characteristics at 300 K, because the sputtering process removes the native oxide layer on the GaAs substrate and forms a clean substrate surface to increase the diode quality. The evaporated SD can be accepted as a nearly ideal diode with the BH of 0.817 eV and ideality factor of 1.102 at 300 K.

Furthermore, the BH value decreases while the ideality factor value increases with a decrease in temperature because the current preferentially flows through the lowest BH with decreasing temperature due to the BH inhomogeneities.[21–25,27,28] Figure 5 shows the experimental effective BHs as a function of the ideality factors for both diodes in the measurement temperature range of 160–300 K, the dashed lines represent the linear least-squares fits to experimental data for each diode. As can be seen from the figure, there is a linear relationship between the effective BHs and ideality factors. Such a dependency is attributed to the lateral inhomogeneity of the BH in the devices.[21–25,27,28]

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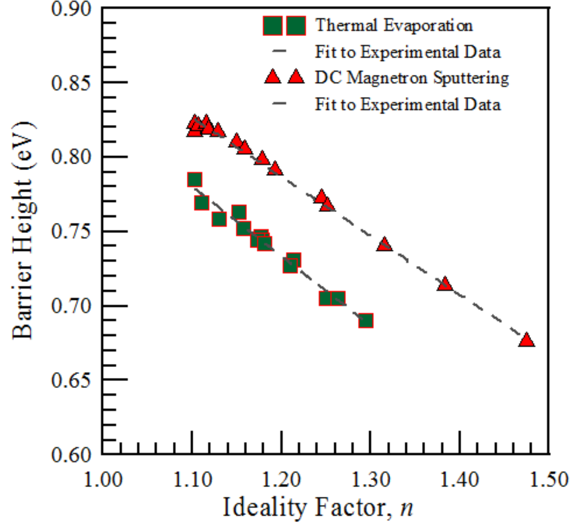

Fig. 5. (Color online) Effective BHs as a function of the ideality factors for both diodes in the measurement temperature range of 160–300 K with steps of 10 K, the dashed line represents the linear least-squares fits to experimental data for each diode.

The reduction in the BHs and the increment in the ideality factor with decreasing measurement temperature have been explained by the lateral distribution of the BH.[24,25,28–50] In such cases, the decrease in the BH with decreasing measurement temperature may obey GD with the mean BH $\bar{\Phi}_b$.[32–34] Figure 6 shows that the apparent BH for the sputtered SD decreases obeying a double GD in the measurement temperature range of 160–300 K. To describe the BH inhomogeneity, the double GD from the multi-GD expression suggested by Jiang *et al.*[32] can be written as

$$\Phi_{\rm ap} = -kT\ln\left[a_1\exp\left(-\frac{\bar{\Phi}_1}{kT}+\frac{\sigma_1^2}{2(kT)^2}\right) + a_2\exp\left(-\frac{\bar{\Phi}_2}{kT}+\frac{\sigma_2^2}{2(kT)^2}\right)\right] \quad (6)$$

The solid line in Fig. 6 represents the fit of Eq. (6) to experimental data. In Eq. (6) and $a_1, a_2, (a_2 = 1 - a_1)$, σ_1, σ_2, and $\bar{\Phi}_1, \bar{\Phi}_2$ are the weight, standard deviation, and mean value of two Gaussian functions, respectively. $\bar{\Phi}_1 = 0.640$ eV, $\bar{\Phi}_2 = 0.855$ eV, $a_2 = 1.20\times10^{-7}$, $\sigma_1 = 70$ mV and $\sigma_2 = 41$ mV were obtained for the sputtered diode. The obtained parameters are given in Fig. 6.

The single GD expression is given by[43–46]

$$\Phi_{\rm ap} = \bar{\Phi}_{b0} - \frac{q\sigma_{s0}^2}{2kT}, \quad (7)$$

where $\Phi_{\rm ap}$ is the zero bias apparent BH or effective BH. The $\Phi_{\rm ap}$ vs $(2kT)^{-1}$ plot according to this expression should be a straight line, whose intercept with the ordinate determines the zero bias mean BH $\bar{\Phi}_{b0}$ and slope gives the zero bias standard deviation σ_{s0}. Figure 7 shows the Φ_{ap} vs $(2kT)^{-1}$ and $(n^{-1}-1)$ vs $(2kT)^{-1}$ plots by means of the single for

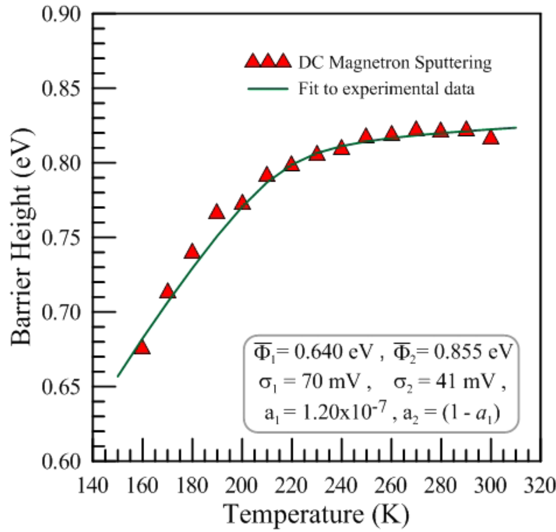

Fig. 6. (Color online) Barrier height vs temperature plot by means of the double GD, in the measurement temperature range of 160–300 K with steps of 10 K, for the Ti/n-GaAs SD prepared by DC magnetron sputtering deposition, the solid line represents the fits to experimental data.

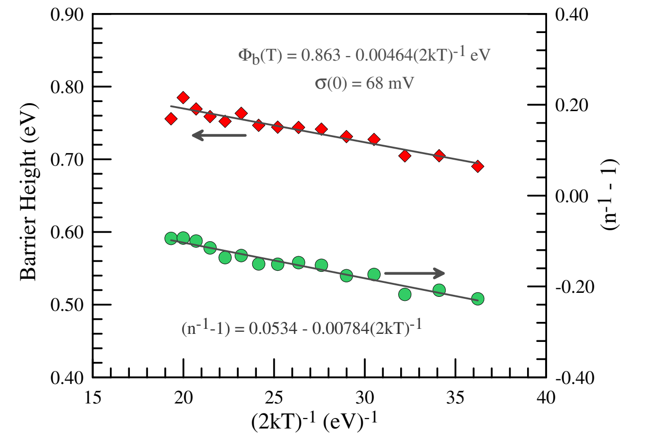

Fig. 7. (Color online) BH vs $(2kT)^{-1}$ and $(n^{-1}-1)$ vs $(2kT)^{-1}$ plots by means of the single GD, in the measurement temperature range of 160–300 K with steps of 10 K, Ti/n-GaAs SD prepared by thermal evaporation deposition, the solid lines represent the fits to experimental data.

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the evaporated SD, in the measurement temperature range of 160–300 K. The intercept and slope of the solid straight line in the Φ_{ap} vs $(2kT)^{-1}$ plot in Fig. 7 gives $\bar{\Phi}_{b0}$ and σ_{s0} values as 0.86 eV and 68 mV for the evaporated SD, respectively.

The linear behavior of $(n^{-1} - 1)$ vs $(2kT)^{-1}$ plot in Fig. 7 demonstrates that the ideality factor expresses the voltage-dependent of the GD of the Schottky BHs. The observed single GD of ideality factor with temperature in the model is given by[44]

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT}, \tag{8}$$

where n_{ap} is apparent ideality factor and the coefficients ρ_2 and ρ_3 quantify the voltage dependence of the BH distribution at the inhomogeneous interface. ρ_2 is the voltage coefficient of the mean BH, and ρ_3 is the voltage coefficient of the standard deviation which are stated by

$$\Delta\bar{\Phi}_b(V,T) = \bar{\Phi}_b(V,T) - \bar{\Phi}_b(0,T) = \rho_2 V, \tag{9}$$

$$\Delta\sigma^2(V) = \sigma^2(V) - \sigma^2(0) = \rho_3 V. \tag{10}$$

Thus, it can be said that this special case where the ideality factor is independent of the bias voltage is valid if the mean BH $\bar{\Phi}_b$ as well as the square of the standard deviation σ^2 vary linearly with the bias. Thus, $\rho_2 = -0.0544\,\text{mV}$ and $\rho_3 = -7.84\,\text{mV}$ values are obtained from the intercept and slope of the straight line of the experimental $(n^{-1} - 1)$ vs $(2kT)^{-1}$ plot in Fig. 7, respectively.

The discrepancies unexpected in the conventional $\ln(I_0/T^2)$ vs $(kT)^{-1}$ plot may be explained according to the GD of the BH. Using Eq. (7) in Eq. (2), it can be rewritten as a modified activation energy expression as follows

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln(AA*) - \frac{q\bar{\Phi}_{b0}}{kT}. \tag{11}$$

The closed circles in Fig. 4 represent a modified $\ln(I_0/T^2) - q^2\sigma_{s0}^2/2(kT)^2$ vs $(kT)^{-1}$ plot for the evaporated SD. The modified experimental data according to Eq. (11) should give a straight line with the slope directly yielding the mean $\bar{\Phi}_{b0}$ and the intercept determining the Richardson constant A^*. The best linear fit of the dashed line to the modified experimental data has given a mean BH $\bar{\Phi}_{b0}$ of 0.86 eV and a Richardson constant A^* of 7.23 $\text{Acm}^{-2}\text{K}^{-2}$ for the evaporated Ti/n-type GaAs SD. This $\bar{\Phi}_{b0}$ has the same value as the mean BHs obtained from the Φ_{ap} vs $(kT)^{-1}$ plot in Fig. 7. The effective Richardson constant of 7.23 $\text{Acm}^{-2}\text{K}^{-2}$ is in close agreement with the value of 8.16 $\text{Acm}^{-2}\text{K}^{-2}$.

4. Conclusion

The sputtered and evaporated Ti/n-type GaAs SDs were made by DC magnetron deposition and by thermal evaporation of Ti on the same n-type GaAs substrates with the ohmic back contact. Information about the electrical behavior of these diodes was obtained from temperature-dependent I–V measurements. The BH and ideality factor values were 0.817 eV and 1.104 for sputtered SDs and 0.756 eV and 1.102 evaporated SDs at 300 K, respectively. It has been seen that the apparent BH values for the diodes have decreased with decreasing temperature, obeying the single-GD for the evaporated diode and the double-GD for the sputtered diode over the whole measurement temperature range. The fact that the BHs distribution for the sputtered diode becomes the double GD may be originated from the sputtering generates defects present in the near-surface region of the semiconductor substrate. We conclude that the thermal evaporation technique yields better quality Schottky contacts for use in electronic devices compared to the DC magnetron deposition technique.

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References

1. L. J. Brillson, *Surf. Sci. Rep.* **2** (1982) 123.
2. S. Sze, *Physics of Semiconductor Devices* (John Wiley & Sons, New York, 1981).
3. E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts* (Clarendon Press, Oxford, 1988).
4. W. R. Wampler and S. M. Myers, *J. Appl. Phys.* **117** (2015) 045707.
5. D. M. Kim, D. H. Kim and S. Y. Lee, *Solid-State Electron.* **51** (2007) 865.
6. A. Cowley and S. Sze, *J. Appl. Phys.* **36** (1965) 3212.
7. M. S. Tyagi, *Surf. Sci.* **64** (1977) 323.
8. J. M. DeLucca, S. E. Mohney, F. D. Auret and S. A. Goodman, *J. Appl. Phys.* **88** (2000) 2593.

9. M. Di Dio, A. Cola, M. Lupo and L. Vanasanelli, *Solid-State Electron.* **38** (1995) 1923.
10. S. Arulkumaran, J. Arokiaraj, N. Dharmarasu and J. Kumar, *Nucl. Instrum. Meth. B.* **119** (1996) 519.
11. G. Myburg, F. D. Auret, W. E. Meyer, C. W. Louw and M. J. van Staden, *Thin Solid Films* **325** (1998) 181.
12. A. Zussman, *J. Appl. Phys.* **59** (1986) 3894.
13. S. Tunhuma, F. Auret, M. Legodi and M. Diale, *Physica B: Condensed Matter* **480** (2016) 201.
14. X. Boddaert, D. Stievenard and J. Bourgoin, *Phys. Rev. B.* **40** (1989) 1051.
15. D. A. Vandenbroucke, R. L. Vanmeirhaeghe, W. H. Laflere and F. Cardon, *Semicond. Sci. Tech.* **2** (1987) 293.
16. R. L. Vanmeirhaeghe, L. M. O. Vandenberghe, W. H. Laflere and F. Cardon, *Solid-State Electron.* **31** (1988) 1629.
17. E. Ayyildiz and A. Türüt, *Solid-State Electron.* **43** (1999) 521.
18. B. Sehgal, V. Balakrishnan and S. Tewari, *JSTS: J. Semicond. Technol. Sci.* **3** (2003) 1.
19. K. Ejderha, S. Duman, C. Nuhoglu, F. Urhan and A.Turut, *J. Appl. Phys.* **116** (2014) 234503.
20. S. K. Cheung and N. W. Cheung, *Appl. Phys. Lett.* **49** (1986) 85.
21. R. T. Tung, *Phys. Rev. B.* **45** (1992) 13509.
22. P. Gammon, A. Pérez-Tomás, V. Shah, O. Vavasour, E. Donchev, J. Pang, M. Myronov, C. A. Fisher, M. Jennings and D. R. Leadley, *J. Appl. Phys.* **114** (2013) 223704.
23. K. Ejderha, A. Zengin, I. Orak, B. Tasyurek, T. Kilinc and A. Türüt, *Mat. Sci. Semicon. Proc.* **14** (2011) 5.
24. A. Akkaya, L. Esmer, T. Karaaslan, H. Cetin and E. Ayyildiz, *Mat. Sci. Semicon. Proc.* **28** (2014) 127.
25. W. Monch, *Appl. Phys. Lett.* **93** (2008) 172118.
26. A. Akkaya, L. Esmer, B. B. Kantar, H. Cetin and E. Ayyildiz, *Microelectron Eng.* **130** (2014) 62.
27. W. Mönch, *Electronic Properties of Semiconductor Interfaces* (Springer, Heidelberg, 2004).
28. A. Akkaya, T. Karaaslan, M. Dede, H. Çetin and E. Ayyildiz, *Thin Solid Films* **564** (2014) 367.
29. R. F. Schmitsdorf, T. U. Kampen and W. Monch, *J. Vac. Sci. Technol. B.* **15** (1997) 1221.
30. B. Boyarbay, H. Çetin, M. Kaya and E. Ayyildiz, *Microelectron. Eng.* **85** (2008) 721.
31. Y. L. Jiang, G. P. Ru, F. Lu and X. P. Qu, *Chin. Phys. Lett.* **19** (2002) 553.
32. Y. L. Jiang, G. P. Ru, F. Lu, X. P. Qu, B. Z. Li and S. Yang, *J. Appl. Phys.* **93** (2003) 866.
33. N. Yildirim, A. Türüt and V. Türüt, *Microelectron. Eng.* **87** (2010) 2225.
34. A. N. Bestas, S. Yazici, F. Aktaş and B. Abay, *Appl. Surf. Sci.* **318** (2014) 280.
35. E. Marıl, A. Kaya, H. G. Çetinkaya, S. Koçyiğit and Ş. Altındal, *Mat. Sci. Semicon. Proc.* **39** (2015) 332.
36. A. Turut, *Turk. J. Phys.* **36** (2012) 235.
37. P. Kaushal and S. Chand, *Int. J. Electron.* **103** (2016) 1.
38. F. Jabli, M. Gassoumi, N. B. Hamadi, M. Charfeddine, T. Alharbi, M. A. Zaidi and H. Maaref, *Silicon* **30** (2015) 12633.
39. H. Çetin and E. Ayyıldız, *Semicond. Sci. Tech.* **20** (2005) 625.
40. N. Elghoul, S. Kraiem, R. Jemai, B. Zebentout and K. Khirouni, *Mat. Sci. Semicon. Proc.* **40** (2015) 302.
41. Z. Çaldıran, Ş. Aydoğan, A. Yesildag, D. Ekinci, S. Kurudirek and A. Türüt, *Mat. Sci. Semicon. Proc.* **34** (2015) 58.
42. Ö. Güllü, M. Biber, S. Duman and A. Türüt, *Appl. Surf. Sci.* **253** (2007) 7246.
43. Y. P. Song, R. L. Vanmeirhaeghe, W. H. Laflere and F. Cardon, *Solid-State Electron.* **29** (1986) 633.
44. J. H. Werner and H. H. Guttler, *J. Appl. Phys.* **69** (1991) 1522.
45. S. Chand and J. Kumar, *Appl. Phys. A* **65** (1997) 497.
46. J. Osvald, *J. Appl. Phys.* **85** (1999) 1935.
47. T. Çakıcı, B. Güzeldir and M. Sağlam, *J. Alloy. Compd.* **646** (2015) 954.
48. N. Kavasoğlu, A. S. Kavasoğlu and B. Metin, *Mater. Res. Bull.* **70** (2015) 804.
49. H. G. Çetinkaya, H. Tecimer, H. Uslu and Ş. Altındal, *Curr. Appl. Phys.* **13** (2013) 1150.
50. S. Alialy, A. Kaya, E. Marıl, S. Altındal and I. Uslu, *Philos. Mag.* **95** (2015) 1448.

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